3 Estimations

The block diagram below illustrates the digital processing path of the XXXXX.

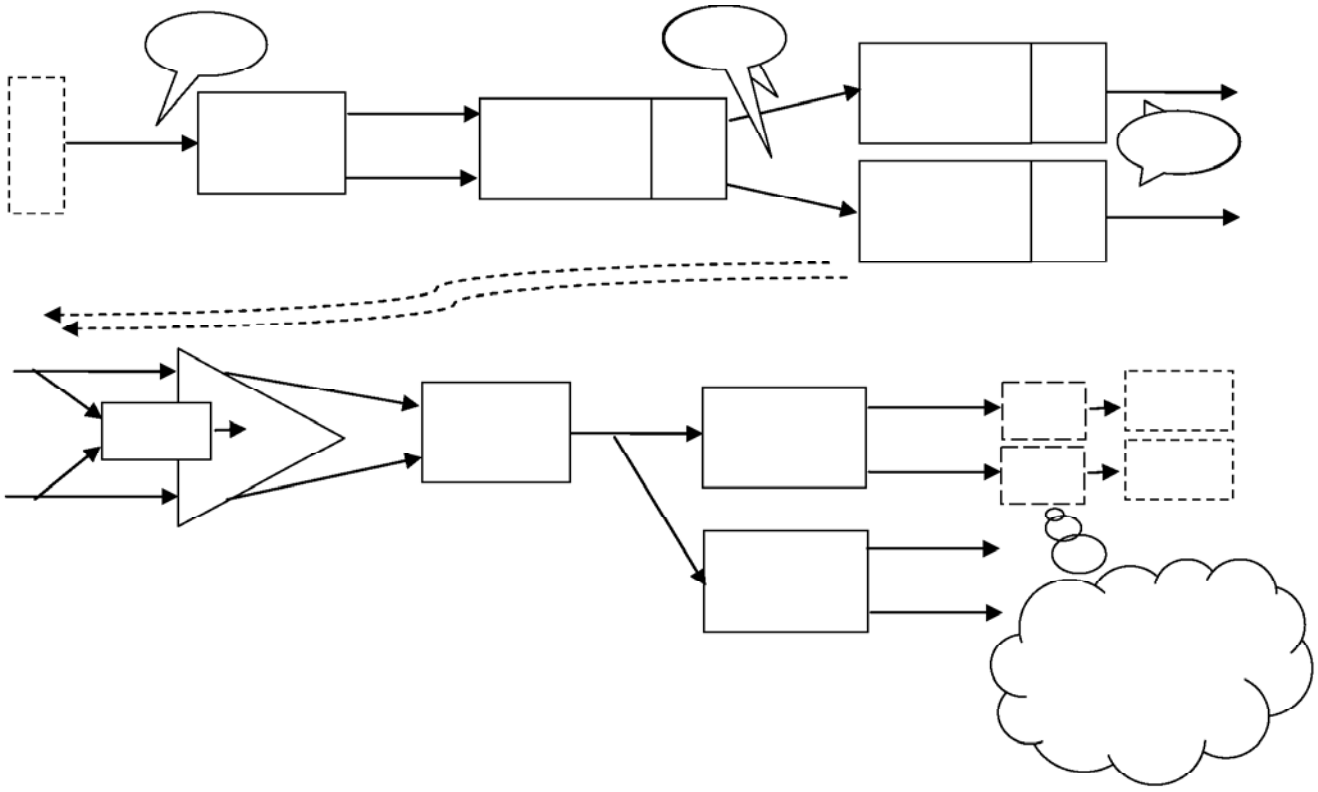

Figure 1 - Block Diagram

Each of the blocks will be discussed in the sections below.

3.1 Phase Rotator & Half Band Filter

The input to the Phase Rotator and Half Band Filter block comes from the ADC at xxxK xx bit samples per second. In this block, the data is decimated by 2, thus two real input samples are consumed and used to generate each I & Q output data pair. Note that the processing rate and the output rate are both xxxK (half the xxxK input rate) due to the decimation by 2. The output samples are xx bits.

3.1.1 Signal processing derivation

The sample frequency is purposely chosen as 4 times the IF rate, so the modulated signal is translated directly to baseband by multiplication with $\exp(i \times 2\pi(-1/4)k)$. This multiplication leads to the following sequences of coefficients for the real input data samples as the I and Q streams are extracted and fed into the filters which follow:

$$\begin{matrix} I \\ Q \end{matrix} : \begin{matrix} 0 & -1 & 0 & 1 & 0 \\ -1 & 0 & 1 & 0 & -1 \end{matrix} \quad \cdots$$

Next, the sequence of input samples is represented as X_n (the current sample), X_{n-1} (the immediately prior sample), etc. and the resultant I and Q data streams for the filters are:

$$\begin{matrix} I \\ Q \end{matrix} : \begin{matrix} -X_{n-10} & 0 & X_{n-8} & 0 & -X_{n-6} & 0 & X_{n-4} & 0 & -X_{n-2} & 0 & X_n \\ 0 & X_{n-9} & 0 & -X_{n-7} & 0 & X_{n-5} & 0 & -X_{n-3} & 0 & X_{n-1} & 0 \end{matrix}$$

The filter coefficients are represented as $\{h_0, h_1, h_2, \ldots, h_{10}\}$. Showing them with the datastreams yields:

$$\begin{matrix} I \\ Q \\ \end{matrix} : \begin{matrix} -X_{n-10} & 0 & X_{n-8} & 0 & -X_{n-6} & 0 & X_{n-4} & 0 & -X_{n-2} & 0 & X_n \\ 0 & X_{n-9} & 0 & -X_{n-7} & 0 & X_{n-5} & 0 & -X_{n-3} & 0 & X_{n-1} & 0 \\ h_{10} & h_9 & h_8 & h_7 & h_6 & h_5 & h_4 & h_3 & h_2 & h_1 & h_0 \end{matrix}$$

Because half band filters are being employed, advantage is taken of a couple of very useful characteristics. The first is that all the odd coefficients $[h_n]$ except the center tap are zero. Applying this yields:

$$\begin{matrix} I \\ Q \\ \end{matrix} : \begin{matrix} -X_{n-10} & 0 & X_{n-8} & 0 & -X_{n-6} & 0 & X_{n-4} & 0 & -X_{n-2} & 0 & X_n \\ 0 & X_{n-9} & 0 & -X_{n-7} & 0 & X_{n-5} & 0 & -X_{n-3} & 0 & X_{n-1} & 0 \\ h_{10} & 0 & h_8 & 0 & h_6 & h_5 & h_4 & 0 & h_2 & 0 & h_0 \end{matrix}$$

Multiplying the Q datastream by the coefficients yields one set of filter computations:

$$\begin{aligned} Q = {} & 0 \times h_{10} + X_{n-9} \times 0 + 0 \times h_8 - X_{n-7} \times 0 + 0 \times h_6 + X_{n-5} \times h_5 + 0 \times h_4 \\ & - X_{n-3} \times 0 + 0 \times h_2 + X_{n-1} \times 0 + 0 \times h_0 \end{aligned}$$

Which simplifies nicely to:

$$Q = 0 + 0 + 0 - 0 + 0 + X_{n-5} \times h_5 + 0 - 0 + 0 + 0 + 0 = X_{n-5} \times h_5$$

With a careful choice of coefficient h_5, and appropriate scaling of all the other coefficients, the Q path filter becomes simply a delay line that produces X_{n-5}. Because there is a decimation by 2, every second sample is unused, resulting in a further simplification of the delay line.

Returning to the I datastream, the other set of filter computations is derived by the multiplication of the appropriate samples by the coefficients:

$$\begin{aligned} I = {} & -X_{n-10} \times h_{10} + 0 \times h_9 + X_{n-8} \times h_8 + 0 \times h_7 - X_{n-6} \times h_6 + 0 \times h_5 + X_{n-4} \times h_4 \\ & + 0 \times h_3 - X_{n-2} \times h_2 + 0 \times h_1 + X_n \times h_0 \end{aligned}$$

This simplifies to:

$$I = -X_{n-10} \times h_{10} + X_{n-8} \times h_8 - X_{n-6} \times h_6 + X_{n-4} \times h_4 - X_{n-2} \times h_2 + X_n \times h_0$$

The second useful property of the halfband filter is now applied. In a halfband filter, the coefficients are symmetrical, thus the identity ax+bx = (a+b)x can be used. By performing the additions in advance of the multiplications, the number of required multiplications is cut in half, as the I filter equation becomes:

$$I = (X_n - X_{n-10}) \times h_{10} + (X_{n-8} - X_{n-2}) \times h_8 + (X_{n-4} - X_{n-6}) \times h_6$$

The decimation by 2 in this block decimates provides another useful characteristic for the hardware. As mentioned above, two real samples are input for processing and used to produce each I & Q output pair. As a result, the zero locations and the non-zero locations in the I and Q paths keep their position with every pass. The impact of this fixed position property is that the zero locations need not be represented in the hardware.

3.1.2 Hardware estimation

The final I and Q filter equations derived above are used to directly realize hardware. The estimated processing for the Half Band Filters is illustrated in the following figure.

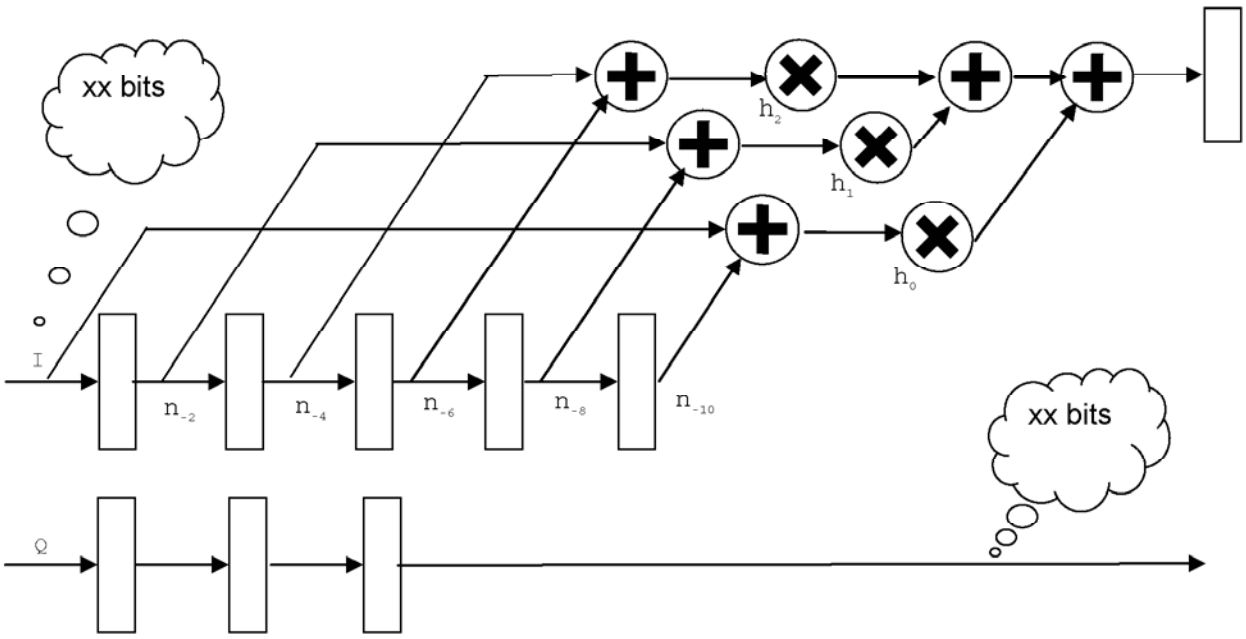

Figure 2 - Half Band Filter

At the required xxxKHz rate, this block needs:

3 Multiply operations

5 Addition operations

9 Delay operations

The estimation is thus: a xx MHz data rate x 3 multiply operations per datum gives a xx MHz operation rate. Multiplying that by an assumed xx bits of data (or coefficient, which ever is smaller) yields xx MHz. This is an acceptable clock rate. The multiplications can thus be implemented with serial-parallel multiplier hardware, which is estimated as 3b cells, being the bit width times 3 (two registers and a full adder per bit). This is much smaller than the b^2 + 4 cells (core plus input & output registers) required by a bxb parallel multiplier.

The area computation is:

$$Area = 6.4 \times 35 \times [\ registers \times \quad bits + \quad mult\_cells \times \quad bits + \ adds \times \quad bits]$$

$$Area = 224 \times [\qquad\qquad\ ] = 224 sq.\mu m / cell \times \qquad cells$$

$$Area = \qquad sq.\mu m$$

The power computation is:

$$Current = \frac{\frac{\mu W}{MHz} \times \qquad MHz \times \qquad cells}{V}$$

$$Current = \frac{\mu W}{V} = \frac{mW}{V} = 0.984 mA$$